HJSIP®

HJ-LPWE5_
Hardware Design Manual

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Preface

Thanks for using the wireless data transmission module provided by HJSIP. HJ-LPWE5 series standard chip-level module, is a high-performance LOT data transceiver. The module adopts LGA package and provides external antenna interface. The product also has the characteristics of low power consumption, small size, strong anti-interference ability, etc., suitable for a variety of application scenarios.

This module is mainly used for data communication, and the company does not assume responsibility for property losses or personal injuries caused by improper operations of users. Please develop the product according to the technical specifications and reference design in the manual. At the same time, pay attention to the general safety matters that should be concerned about when using mobile products.

Before the announcement, the company has the right to modify the content of this manual according to the needs of technological development.

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Contents

Version History

Version	Date	Change Description	Reviser	Reviewer
V1.0	2024/09/05	Initial Version	LMY	LJH
V1.1	2025/02/14	updated parameter	WYW	LMY

Applicable module selection

No.	Module type	Type	Description
1	HJ-LPWE5-P 400	STM32WLE5，410MHZ-525MHZ，Passive 32MHZ crystal oscillator	The core uses the STM32WLE5 scheme, the radio frequency is matched to the frequency range of 410-525MHZ, passive crystal oscillator
2	HJ-LPWE5-P 800	STM32WLE5，800MHZ-950MHZ，Passive 32MHZ crystal oscillator	The core uses the STM32WLE5 scheme, the radio frequency is matched to the frequency range of 800-950MHZ, and the passive crystal oscillator
3	HJ-LPWE5-A 400	STM32WLE5，410MHZ-525MHZ，Active TCXO thermocompensating oscillator 32MHZ	The core uses the STM32WLE5 scheme, the radio frequency is matched to the frequency range of 410-525MHZ,Active TCXO thermocompensating oscillator
4	HJ-LPWE5-A 800	STM32WLE5，800MHZ-950MHZ，Active TCXO thermocompensating oscillator 32MHZ	The core uses the STM32WLE5 scheme, the radio frequency is matched to the frequency range of 800-950MHZ,Active TCXO thermocompensating oscillator

1 introduction

The HJ-LPWE5 is a general-purpose LPWAN SoC based on the single-core Arm Cortex-M4/M0+ architecture that supports LoRa communication.

The module specifications support two types: ordinary passive crystal style and TCXO temperature compensation crystal style.

Ideally, the sensitivity can reach -148dBm, the maximum transmission power +22dBm, and the user can control the internal MCU through ARM programming and development software such as KEIL to achieve wireless data transmission and receiving. Please refer to STM32WL55 datasheet for more details.

2 Product overview

2.1 Key features

Table 2-1：HJ-LPWE5 key characteristics

Characteristic	Description
function	- Built-in 256KB FLASH and 64KB RAM - 32MHz passive crystal oscillator or TCXO is available internally - Contains 32.768KHz crystal oscillator
frequency range	Free frequency bands 410MHZ-525MHZ or 800MHZ-950MHZ are available without application
Modulation Mode	Support LoRa，(G)FSK，(G)MSK and BPSK
transmitting power	Maximum transmitting power: +22dBm
sensitivity	-148dBm
supply voltage	Single power supply wide voltage supply
operating current	-TX Peak current(LoRa): 15mA(@+10dBm)；110.5mA（@+22dBm） -RX Peak current:4.82mA
low-power dissipation	Low power standby: 360nA (32KB RAM reserved, RTC not turned off) 31nA in ultra-low power mode (RF/MCU function removed, RTC off)
Size	7.5mm * 7.5mm * 1.1mm（L*W*H）

2.2 application scenarios

- Smart home wireless remote control, data transmission
- Wireless POS machine
- Industrial control, three types of instruments wireless communication
- Other wireless, low power applications
- LoRaWAN,LinkWAN application

2.3 functional block diagram

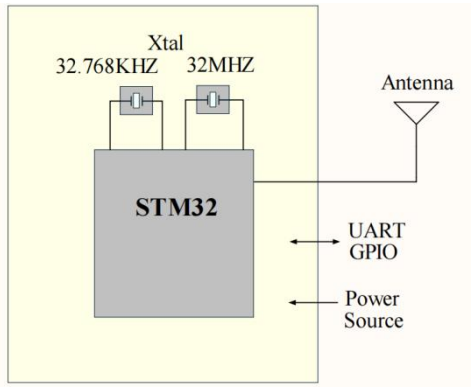


Figure 2.1：HJ-LPWE5 functional block diagram

2.4 Pins distribution diagram

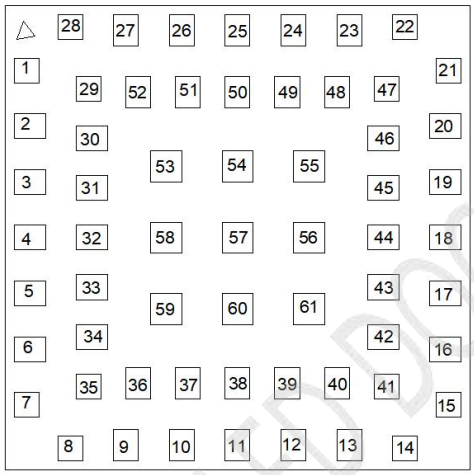


Figure 2.2：HJ-LPWE5 Pins distribution diagram

2.5 Pins description table

Table 2-2：HJ-LPWE5 Pins definition table

PIN	Name	Type	Description	Remarks
1	RFO_HP	O	RF High power output	For high power RF output, connect to RFO_IN pin
2	PA6	IO	Universal IO port	/
3	VDD_TCXO/PB0	POWER/IO	TCXO power supply/Universal IO port	/
4	PA9	IO	Universal IO port	/
5	PB12	IO	Universal IO port	/
6	PB13	IO	Universal IO pout	/
7	PA11	IO	Universal IO port	/
8	PA13	IO	Universal IO port	/
9	VBAT	POWER	Backup power input	1.55-3.6V, when VDD is not present, power the RTC/TAMP/ external 32kHz crystal and backup register.
10	OSC32_IN /PC14	OSC32_IN/IO	32.768K crystal oscillator input/Universal IO	Not use the internal crystal oscillator, it can be used as a general purpose IO port

			port	
11	OSC32_OUT/PC15	OSC32_OUT/IO	32.768K crystal oscillator output/Universal IO port	Not use the internal crystal oscillator, it can be used as a general purpose IO port
12	VREF+	POWER	Reference voltage input	The input reference voltage of the ADC and DAC, is also the output of the internal reference voltage buffer
13	PC5	IO	Universal IO port	/
14	PB15	IO	Universal IO port	/
15	PB7	IO	Universal IO port	/
16	PB4	IO	Universal IO port	/
17	PB3	IO	Universal IO port	/
18	PB5	IO	Universal IO port	/
19	PB6	IO	Universal IO port	/
20	PC1	IO	Universal IO port	/
21	PA3	IO	Universal IO port	/
22	RF_PIN	RF out	External antenna output	External antenna access
23	GND	IO	Universal IO port	/
24	PA4	IO	Universal IO port	/
25	PA8	IO	Universal IO port	/
26	BOOT0/PH3	IO	Universal IO port	/
27	RFO_LP	O	RF Low power output	For a low power output RF signal, connect to the RFO_IN pin
28	RFO_IN	I	RF Output signal input source	Selective connect RFO_HP or RFO_LP
29	PB11	IO	Universal IO port	/
30	PC4	IO	Universal IO port	/
31	NRST	RESET	Reset Pin	Low level effective
32	PB1	IO	Universal IO port	/
33	PB2	IO	Universal IO port	/
34	PA10	IO	Universal IO port	/
35	PA0	IO	Universal IO port	/
36	PA12	IO	Universal IO port	/
37	PC13	IO	Universal IO port	/
38	PB14	IO	Universal IO port	/
39	PC3	IO	Universal IO port	/
40	PA14	IO	Universal IO port	/
41	PB9	IO	Universal IO port	/
42	PA15	IO	Universal IO port	/
43	PC2	IO	Universal IO port	/
44	PB8	IO	Universal IO port	/
45	PC0	IO	Universal IO port	/
46	PA2	IO	Universal IO port	/
47	GND	POWER	Power Supply GND	/
48	PA5	IO	Universal IO port	/
49	PA7	IO	Universal IO port	/
50	PB10	IO	Universal IO port	/
51	PC6	IO	Universal IO port	/
52	PA1	IO	Universal IO port	/

53	GND	POWER	Power Supply GND	/
54	GND	POWER	Power Supply GND	/
55	GND	POWER	Power Supply GND	/
56	GND	POWER	Power Supply GND	/
57	GND	POWER	Power Supply GND	/
58	GND	POWER	Power Supply GND	/
59	VDD	POWER	Power Input	1.8-3.6V
60	VDD	POWER	Power Input	1.8-3.6V
61	VDDA	POWER	analog power	External analog power supply for A/D, D/A converters、voltage reference buffers and comparators. 0 V to 3.6 V

Table 2-3：GPIO peripheral function list

GPIO No.	Vicarious function	Additional function
PA0	TIM2_CH1, I2C3_SMBA, I2S_CKIN, USART2_CTS, COMP1_OUT, DEBUG_PWR_REGLP1S, TIM2_ETR,CM4_EVENTOUT	TAMP_IN2/WKUP1
PA1	TIM2_CH2,LPTIM3_OUT,I2C1_SMBA,SPI1_SCK, USART2_RTS,LPUART1_RTS,DEBUG_PWR_REGLP2S, CM4_EVENTOUT	/
PA2	LSCO,TIM2_CH3,USART2_TX,LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT	LSCO
PA3	TIM2_CH4,I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT	/
PA4	RTC_OUT2,LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_ NSSOUT,LPTIM2_OUT, CM4_EVENTOUT	/
PA5	TIM2_CH1,TIM2_ETR,SPI2_MISO,SPI1_SCK, DEBUG_SUBGHZSPI_ SCKOUT,LPTIM2_ETR, CM4_EVENTOUT	/
PA6	TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_MISOOUT, TIM16_CH1, CM4_EVENTOUT	/
PA7	TIM1_CH1N,I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_MOSIOUT,TIM17_CH1, CM4_EVENTOUT	/
PA8	MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT,CM4_EVENTOUT	/
PA9	TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX,CM4_EVENTOUT	/
PA10	RTC_REFIN,TIM1_CH3, I2C1_SDA, SPI2_MOSI/I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INM, COMP2_INM, DAC_OUT1, ADC_IN6
PA11	TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO,USART1_CTS,DEBUG_RF_NRESET,CM4_EVENTOUT	COMP1_INM,COMP2_INM, ADC_IN7
PA12	TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT	ADC_IN8
PA13	JTMS-SWDIO,I2C2_SMBA, IR_OUT, CM4_EVENTOUT	ADC_IN9
PA14	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	ADC_IN10
PA15	JTDI,TIM2_CH1,TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT	COMP1_INM, COMP2_INP, ADC_IN11

PB0/VDD TCXO	COMP1_OUT, CM4_EVENTOUT	/
PB1	LPUART1_RTS_DE,LPTIM2_IN1,CM4_EVENTOUT	COMP2_INP,ADC_IN5
PB2	LPTIM1_OUT,I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSRDY, CM4_EVENTOUT	COMP1_INP, COMP2_INM, ADC_IN4
PB3	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, DEBUG_RF_DTB1, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN2, TAMP_IN3/WKUP3
PB4	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INP, COMP2_INP, ADC_IN3
PB5	LPTIM1_IN1,I2C1_SMBA, SPI1_MOSI,RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN,CM4_EVENTOUT	/
PB6	LPTIM1_ETR,I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT	/
PB7	LPTIM1_IN2,TIM1_BKIN, I2C1_SDA,USART1_RX, TIM17_CH1N, CM4_EVENTOUT	/
PB8	TIM1_CH2N,I2C1_SCL, RF_IRQ2,TIM16_CH1, CM4_EVENTOUT	/
PB9	TIM1_CH3N,I2C1_SDA, SPI2_NSS/I2S2_WS,IR_OUT, TIM17_CH1, CM4_EVENTOUT	/
PB10	TIM2_CH3,I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT	/
PB11	TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT	/
PB12	TIM1_BKIN,I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT	/
PB13	TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT	ADC_IN0
PB14	TIM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT	ADC_IN1
PB15	TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT	/
PC0	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT	/
PC1	LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT	/
PC2	LPTIM1_IN2,SPI2_MISO, CM4_EVENTOUT	/
PC3	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, LPTIM2_ETR, CM4_EVENTOUT	/
PC4	CM4_EVENTOUT	/
PC5	CM4_EVENTOUT	/
PC6	I2S2_MCK, CM4_EVENTOUT	/
PC13	CM4_EVENTOUT	TAMP_IN1/ RTC_OUT1/RTC_TS/ WKUP2
PC14/OSC32_IN	CM4_EVENTOUT	OSC32_IN
PC15/OSC32_OUT	CM4_EVENTOUT	OSC32_OUT
PH3/BOOT0	CM4_EVENTOUT	BOOT0

Table 2-4：GPIO peripheral function mapping table

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART 1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17 LPTIM2	EVENOUT
Port A	PA0	-	TIM2_ CH1	-	-	I2C3_ SMBA	I2S_ CKIN	-	USART2 _CTS	-	-	-	-	COMP1_ OUT	DEBUG_PWR_REGLP1 S	TIM2_ETR	CM4_EVE NTOUT
	PA1	-	TIM2_ CH2	-	LPTIM3_ OUT	I2C1_ SMBA	SPI1_ SCK	-	USART2 _RTS	LPUART 1_RTS	-	-	-	-	DEBUG_PWR_REGLP2 S	-	CM4_EVE NTOUT
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	USART2 _TX	LPUART 1_TX	-	-	-	COMP2_ OUT	DEBUG_PWR_LDORD Y	-	CM4_EVE NTOUT
	PA3	-	TIM2_ CH4	-	-	-	I2S_ MCK	-	USART2 _RX	LPUART 1_RX	-	-	-	-	-	-	CM4_EVE NTOUT
	PA4	RTC_ OUT2	LPTIM1 _OUT	-	-	-	SPI1_ NSS	-	USART2 _CK	-	-	-	-	-	DEBUG_ SUBGHZSPI_NSSOUT	LPTIM2_ OUT	CM4_EVE NTOUT
	PA5	-	TIM2_ CH1	TIM2_ ETR	SPI2_ MISO	-	SPI1_ SCK	-	-	-	-	-	-	-	DEBUG_ SUBGHZSPI_SCKOUT	LPTIM2_ ETR	CM4_EVE NTOUT
	PA6	-	TIM1_ BKIN	-	-	I2C2_ SMBA	SPI1_ MISO	-	-	LPUART 1_CTS	-	-	-	TIM1_ BKIN	DEBUG_ SUBGHZSPI_MISOOU T	TIM16_ CH1	CM4_EVE NTOUT
	PA7	-	TIM1_ CH1N	-	-	I2C2_ SCL	SPI1_ MOSI	-	-	-	-	-	-	COMP2_ OUT	DEBUG_ SUBGHZSPI_MOSIOU T	TIM17_ CH1	CM4_EVE NTOUT
	PA8	MCO	TIM1_ CH1	-	-	-	SPI2_ SCK/ I2S2_CK	-	USART1 _CK	-	-	-	-	-	-	LPTIM2_ OUT	CM4_EVE NTOUT
	PA9	-	TIM1_ CH2	-	SPI2_NSS /I2S2_WS	I2C1_ SCL	SPI2_ SCK/ I2S2_CK	-	USART1 _TX	-	-	-	-	-	-	-	CM4_EVE NTOUT
	PA10	RTC_ REFIN	TIM1_ CH3	-	-	I2C1_ SDA	SPI2_ MOSI/ I2S2_SD	-	USART1 _RX	-	-	-	-	-	DEBUG_RF_ HSE32RDY	TIM17_ BKIN	CM4_EVE NTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	LPTIM3_ ETR	I2C2_ SDA	SPI1_ MISO	-	USART1 _CTS	-	-	-	-	TIM1_ BKIN2	DEBUG_RF_ NRESET	-	CM4_EVE NTOUT
	PA12	-	TIM1_ ETR	-	LPTIM3_ IN1	I2C2_ SCL	SPI1_ MOSI	RF_ BUSY	USART1 _RTS	-	-	-	-	-	-	-	CM4_EVE NTOUT
	PA13	JTMS-SWDIO	-	-	-	I2C2_ SMBA	-	-	-	IR_OUT	-	-	-	-	-	-	CM4_EVE NTOUT
	PA14	JTCK-SWCLK	LPTIM1 _OUT	-	-	I2C1_ SMBA	-	-	-	-	-	-	-	-	-	-	CM4_EVE NTOUT
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-	I2C2_ SDA	SPI1_ NSS	-	-	-	-	-	-	-	-	-	CM4_EVE NTOUT

Table 2-4：GPIO peripheral function mapping table（continued）

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART 1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17 LPTIM2	EVENOUT
Port B	PB0	-	-	-	-	-	-	-	-	-	-	-	-	COMP1_ OUT	-	-	CM4_EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART 1_ RTS_DE	-	-	-	-	-	LPTIM2 _ IN1	CM4_EVENTOUT
	PB2	-	LPTIM1_OUT	-	-	I2C3_ SMBA	SPI1_ NSS	-	-	-	-	-	-	-	DEBUG_RF_ SMPSRDY	-	CM4_EVENTOUT
	PB3	JTDO/ TRACE SWO	TIM2_ CH2	-	-	-	SPI1_ SCK	RF_IRQ0	USART1_RTS	-	-	-	-	-	DEBUG_RF_ DTB1	-	CM4_EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_ SDA	SPI1_ MISO	-	USART1_CTS	-	-	-	-	-	DEBUG_RF_ LDORDY	TIM17_ BKIN	CM4_EVENTOUT
	PB5	-	LPTIM1_ IN1	-	-	I2C3_ SMBA	SPI1_ MOSI	RF_IRQ1	USART1_CK	-	-	-	-	COMP2_ OUT	-	TIM16_ BKIN	CM4_EVENTOUT
	PB6	-	LPTIM1_ETR	-	-	I2C1_ SCL	-	-	USART1_TX	-	-	-	-	-	-	TIM16_ CH1N	CM4_EVENTOUT
	PB7	-	LPTIM1_ IN2	-	TIM1_ BKIN	I2C1_ SDA	-	-	USART1_RX	-	-	-	-	-	-	TIM17_ CH1N	CM4_EVENTOUT
	PB8	-	TIM1_ CH2N	-	-	-	-	RF_IRQ2	-	-	-	-	-	-	-	TIM16_ CH1	CM4_EVENTOUT
	PB9	-	TIM1_ CH3N	-	-	I2C1_ SDA	SPI2_ NSS/ I2S2_WS	-	-	IR_OUT	-	-	-	-	-	TIM17_ CH1	CM4_EVENTOUT
	PB10	-	TIM2_ CH3	-	-	I2C3_ SCL	SPI2_ SCK/ I2S2_CK	-	-	LPUART 1_RX	-	-	-	COMP1_ OUT	-	-	CM4_EVENTOUT
	PB11	-	TIM2_ CH4	-	-	I2C3_ SDA	-	-	-	LPUART 1_TX	-	-	-	COMP2_ OUT	-	-	CM4_EVENTOUT
	PB12	-	TIM1_ BKIN	-	TIM1_ BKIN	I2C3_ SMBA	SPI2_ NSS/ I2S2_WS	-	-	LPUART 1_RTS	-	-	-	-	-	-	CM4_EVENTOUT
	PB13	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI2_ SCK/ I2S2_CK	-	-	LPUART 1_CTS	-	-	-	-	-	-	CM4_EVENTOUT
	PB14	-	TIM1_ CH2N	-	I2S2_ MCK	I2C3_ SDA	SPI2_ MISO	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PB15	-	TIM1_ CH3N	-	-	I2C2_ SCL	SPI2_ MOSI/ I2S2_SD	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT

Table 2-4：GPIO peripheral function mapping table（continued）

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART 1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17 LPTIM2	EVENOUT
Port C	PC0	-	LPTIM1_ IN1	-	-	I2C3_ SCL	-	-	-	LPUART 1_RX	-	-	-	-	-	LPTIM2 _ IN1	CM4_EVENTOUT
	PC1	-	LPTIM1_ OUT	-	SPI2_ MOSI/ I2S2_SD	I2C3_ SDA	-	-	-	LPUART 1_TX	-	-	-	-	-	-	CM4_EVENTOUT
	PC2	-	LPTIM1_ IN2	-	-	-	SPI2_ MISO	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC3	-	LPTIM1_ ETR	-	-	-	SPI2_ MOSI/ I2S2_SD	-	-	-	-	-	-	-	-	LPTIM2 _ ETR	CM4_EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC6	-	-	-	-	-	I2S2_ MCK	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PB13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PB14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PB15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
Port H	PH3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT

3 Electrical Parameters

3.1 Absolute Maximum Ratings

Table 3-1：Absolute Maximum Ratings

Parameter	MIN	MAX	Unit
supply voltage VCC	1.7	3.9	V
IO Supply Voltage	0	VCC	V
Operating Temperature	-40	+85	℃
Storage Temperature	-55	+125	℃

3.2 DC Characteristics

Table 3-2：Recommended Operating Conditions

Parameter	MIN	TYP	MAX	Unit
Supply voltage VCC	1.8	3.3	3.6	V
IO Supply Voltage	0	3.3	VCC	V
Dormant working current	/	0.36	/	uA
Maximum Operating Current@+22dBm	/	110.5mA(434-490MHz) 120mA(868-915MHz)	/	mA
Operating Temperature	-40	+25	+85	℃

4 RF Features

The module sets the external antenna interface.

Table 4-1：RF features

Attribute	Value	Remarks
Wireless modulation mode	GFSK、FSK、LORA,etc	/
Frequency range	410-525Mhz 或 800-950Mhz	/
Air speed	0.013Kbps - 17.4Kbps(LoRa) 0.6Kbps - 300Kbps（FSK）	/
Transmit Power	MAX . +22dbm	/
Receive sensitivity	MAX.-148dbm	/
antenna	External antenna	/

5 Announcements

5.1 Notices for Hardware Design

- It is recommended to use a dedicated antenna that matches the specifications of the wireless frequency band, such as a spring antenna.
- The module antenna should be placed around the edge of the circuit board, the antenna part is

close to the edge or corner of the main board, it is best to place the module in the corner of the circuit board.

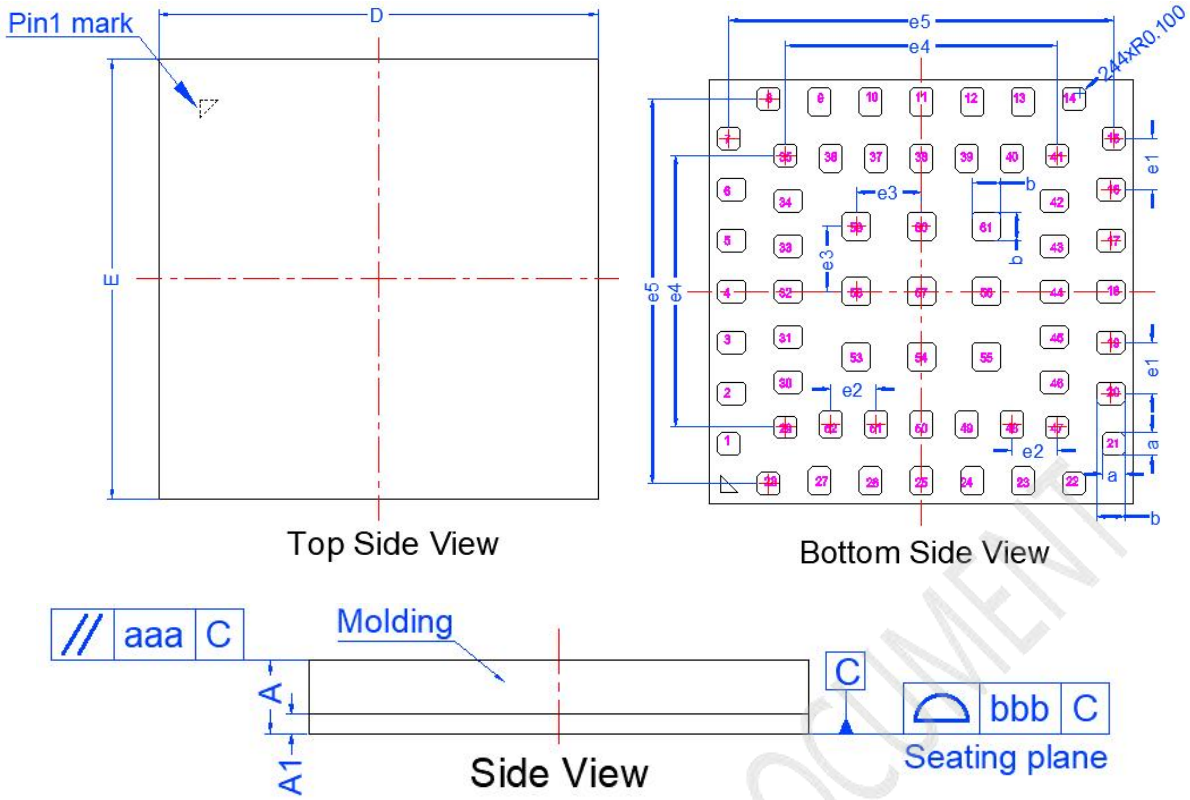
- Do not place other components near or on the back of the antenna of the wireless module and do not route cables. Placing devices or wiring will affect wireless performance.
- Each layer of the circuit board should be covered with copper for GND connection, and the copper covering area of the module, especially the antenna part, should be large enough and well grounded.
- Holes must be drilled in the copper-covered area of the entire circuit board, especially in the vicinity of the module and antenna.
- If space permits, it is best to reserve a π filter circuit between the module and the antenna.
- If there are high-power devices or high-voltage conversion circuits on the circuit board, separate the GND copper covering of the modules from those of other parts, connect the modules to the ground ground in a single point, and connect holes as many as possible to reduce interference on radio signals.
- Modules should not be placed in metal housing, if a metal housing must be used then the antenna must be removed.
- If the wireless module is to be installed, keep metal components, such as screws and inductors, away from the radio antenna of the wireless module.
- The input power supply is recommended to be filtered by magnetic beads or inductance. The filter capacitors C1 and C2 should be placed as close as possible to the power input pin of the module.
- All pins please pay attention to the pin diagram, and the IO connected to it please pay attention to the IO mode and status. If there is enough space when the serial port is connected to the MCU, it is best to add a 100 ohm resistor.
- GND Must be well grounded.
- Unwanted pins can be suspended.

5.2 Precautions for ultrasonic welding

Please carefully consider using ultrasonic welding technology. If it is necessary to use ultrasonic welding technology, please use 40KHz high frequency ultrasound welding technology. Keep the module away from the ultrasonic soldering line and the fixing column during the design method to prevent damage to the module!

For specific ultrasonic welding matters, please contact our company for technical consultation.

6 Dimension figure



DIMENSIONAL REFERENCES *Units:mm*

SYMBOL	DIMENSIONAL REQMTS			SYMBOL	Tolerance of Form &Position
	MIN	NOM	MAX	aaa	0.10
A	1.06	1.10	1.14	bbb	0.10
A1	0.27	0.30	0.33		
D	7.40	7.50	7.60		
E	7.40	7.50	7.60		
a	0.35	0.40	0.45		
b	0.45	0.50	0.55		
e1	0.90REF.				
e2	0.80REF.				
e3	1.15REF.				
e4	4.80REF.				
e5	6.80REF.				

Note:
1. All dimensions are in mm

Figure 6.1：HJ-LPWE5 Mechanical dimensional drawing

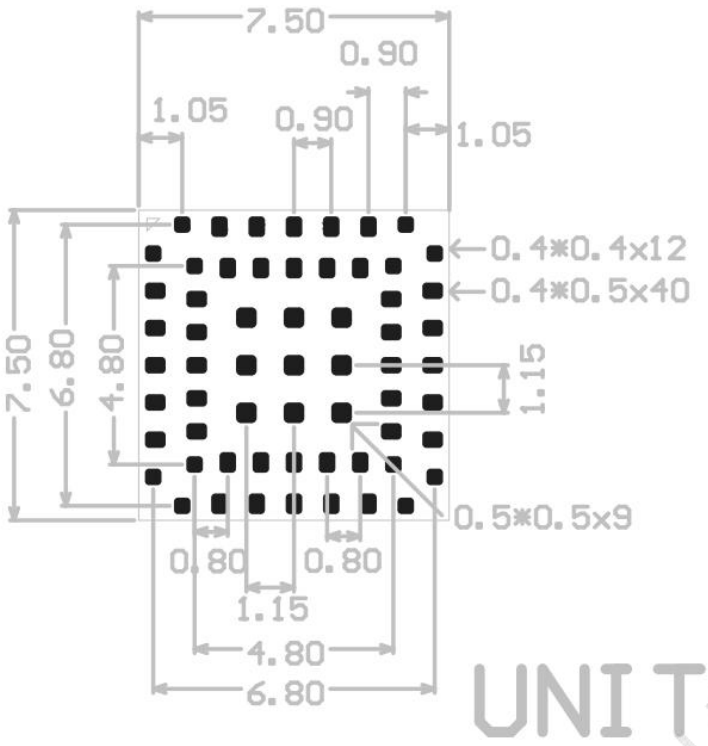


Figure 6.2：HJ-LPWE5 Package size drawing

7 Soldering Recommendations

HJ-LPWE5 module use high temperature resistant materials, manufacturing by Lead-free Process. The maximum temperature resistance is 265℃. Ten continuous reflow soldering has no effect on properties and strength. Specific parameters as shown in Table 7-1.

Table 7-1：Reflow soldering parameters

Parameter	Value
Features	Lead-free process
Average ramp up rate(T_{SMAX} to Tp)	max3℃/sec. max
Temperature Min($T_S$min)	150℃
Temperature Max(TSmax)	200℃
Preheat time (Min to Max) (tS)	80~100sec
Peak Temperature (T_P)	250±5℃
Ramp-down Rate	6℃/sec. max
Time 25℃ to Peak Temp (T_P)	8 min. max

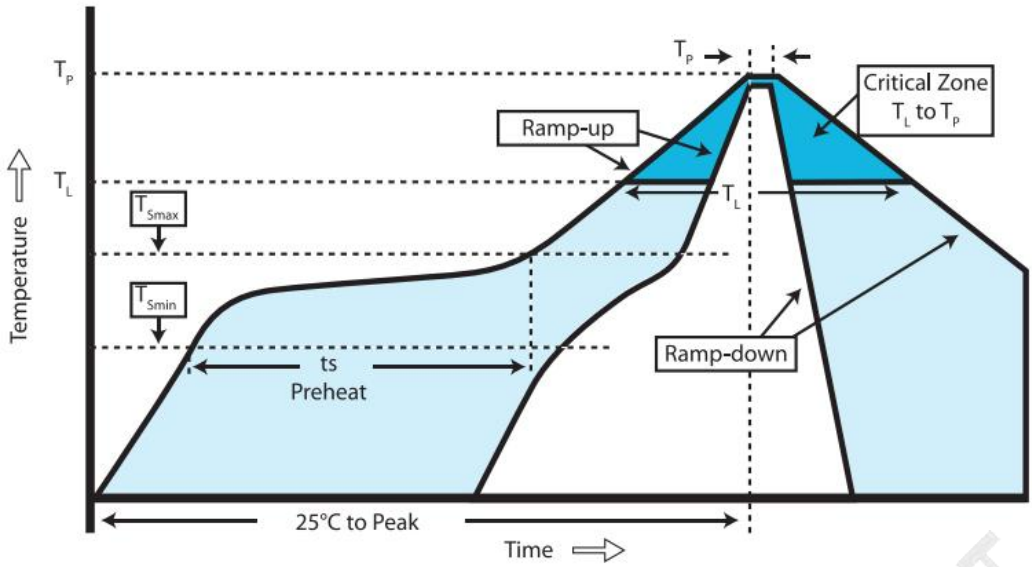


Figure 7.1：Temperature Curve of Reflow Welding

8 Packaging

8.1 Packaging method

Table 8-1：Packaging method

Type	Packaging method
HJ-LPWE5-xxx	Roll tape

Use chip-grade anti-static aluminum foil bags to seal and pack with braid. Each bag is put in desiccant. Industrial grade vacuum pump ensures no air leakage, moisture, water and dust (IP65). The actual packaging effect is shown in Figure 8.1.

Figure 8.1：package figure

8.2 Label information

All packages are labeled with cargo information, ROHS label, anti-static label, etc.

【A】Tangshan Hongjia electronic Technology Co., LTD
【B】HJ-XXX-XXX
【C】Pb Free Reflow(260℃)
【D】Date Code:2508 HJ0218
【E】Note: Must be stored in a vacuum Seal
【F】Warning: Humidity sensitivity level MSL:XX
【G】QTY:1500PCS SEAL DATE:20250218

Figure 8.2：Product label drawing

Table 8-2：Module information description

No.	Description
A	company name
B	product model
C	Lead-free reflow mark and reflow temperature setting value
D	Production date Example: 2508 HJ0218 represents the product produced in the 8th week of 2025, on February 18
E	Storage precautions
F	Humidity sensitivity level
G	Quantity of product + date of sale